

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

TRANSMITTAL FORM (to be used for all correspondence after initial filing)		Application Number	10/622,314
		Filing Date	July 17, 2003
		First Named Inventor	Wang, Bonnie I.
		Art Unit	2811
		Examiner Name	To Be Assigned
Total Number of Pages in This Submission	7	Attorney Docket Number	015114-066800US

ENCLOSURES (Check all that apply)

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	Townsend and Townsend and Crew LLP Steven Cahill	Reg. No. 44,578
Signature	<i>Steven Cahill</i>	
Date	March <u>10</u> , 2004	

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PATENT
Attorney Docket No.: 015114-066800US
Client Reference No.: A1030

On 3-12-04



TOWNSEND and TOWNSEND and CREW LLP

By: Edward Masinas
EDWARD MASINAS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Bonnie I. Wang et al.

Application No.: 10/622,314

Filed: July 17, 2003

For: PROGRAMMABLE ON-CHIP
DIFFERENTIAL TERMINATION
IMPEDANCE

Examiner: To Be Assigned

Art Unit: 2811

INFORMATION DISCLOSURE
STATEMENT UNDER 37 CFR §1.97 and
§1.98

Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of Reference Nos. 56-64 are enclosed herewith. Reference Nos. 1-55 are not enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

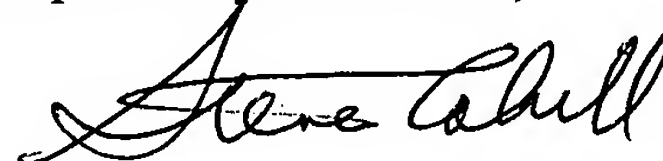
As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no

representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement.

However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

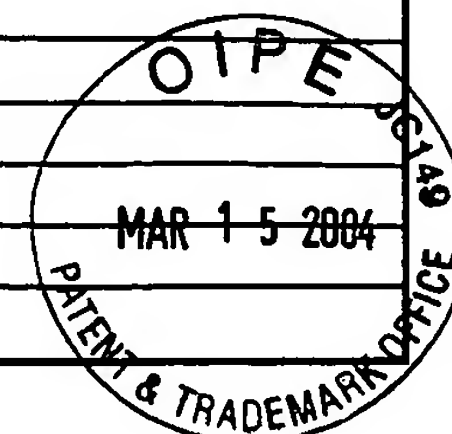
Respectfully submitted,



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60161638 v1

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>			Complete if Known		
			Application Number	10/622,314	
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			Art Unit	2811	
Examiner Name	To Be Assigned				
Attorney Docket Number	015114-066800US				
Sheet	1	of	3		



U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	0001	US-4,719,369	01-12-1988	Asano et al.	
	0002	US-4,954,729	09-04-1990	Urai	
	0003	US-5,111,081	05-05-1992	Atallah	
	0004	US-5,134,311	07-28-1992	Biber et al.	
	0005	US-5,164,663	11-17-1992	Alcorn	
	0006	US-5,179,300	01-12-1993	Rolandi et al.	
	0007	US-5,359,235	10-25-1994	Coyle et al.	
	0008	US-5,374,861	12-20-1994	Kubista	
	0009	US-5,592,510	01-07-1997	Van Brunt et al.	
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	0011	US-5,623,216	04-22-1997	Penza et al.	
	0012	US-5,726,582	03-10-1998	Hedberg	
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	0015	US-5,864,715	01-26-1999	Zani et al.	
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	0018	US-5,970,255	10-19-1999	Tran et al.	
	0019	US-6,008,665	12-28-1999	Kalb et al.	
	0020	US-6,026,456	02-15-2000	Ilkbahar	
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	0022	US-6,049,255	04-11-2000	Hagberg et al.	
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	0025	US-6,097,208	08-01-2000	Okajima et al.	
	0026	US-6,100,713	08-08-2000	Kalb et al.	
	0027	US-6,118,310	09-12-2000	Esch, Jr.	
	0028	US-6,147,520	11-14-2000	Kothandaraman et al.	
	0029	US-6,154,060	11-28-2000	Morriss	
	0030	US-6,157,206	12-05-2000	Taylor et al.	
	0031	US-6,181,157 B1	01-30-2001	Fiedler	
	0032	US-6,236,231 B1	05-22-2001	Nguyen	
	0033	US-6,252,419 B1	06-26-2001	Sung et al.	

Examiner Signature		Date Considered	
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60161638 v1

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	0034	US-6,329,836 B1	12-11-2001	Drost et al.	
	0035	US-6,356,106 B1	03-12-2002	Greeff et al.	
	0036	US-6,362,644 B1	03-26-2002	Jeffrey et al.	
	0037	US-6,366,128 B1	04-02-2002	Ghia et al.	
	0038	US-6,411,126 B1	06-25-2002	Tinsley et al.	
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	0041	US-6,433,579 B1	08-13-2002	Wang et al.	
	0042	US-6,445,245 B1	09-03-2002	Schultz et al.	
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	0049	US-6,639,397 B2	10-28-2003	Roth et al.	
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	0051	US 2002/0010853 A1	01-24-2002	Trimberger et al.	
	0052	US 2002/0060602 A1	05-23-2002	Ghia et al.	
	0053	US 2002/0101278 A1	08-01-2002	Schultz et al.	
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	0055	US 2004/0008054 A1	01-15-2004	Lesea et al.	

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Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
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				Art Unit	2811
				Examiner Name	To Be Assigned
Sheet	3	of	3	Attorney Docket Number	015114-066800US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	0056	Altera, Apex 20K "Programmable Logic Device Family," Altera Corporation, Ver. 1.1, May 2001	
	0057	Altera, Apex II "Programmable Logic Device Family," Altera Corporation, Ver. 1.1, May 2001	
	0058	Bendak, M. et al. (1996). "CMOS VLSI Implementation of Gigabyte/second computer network links," Dept. of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093-0407, IEEE <i>International Symposium on Circuits and Systems</i> pp.269-272.	
	0059	Boni, A. et al. (2001). "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-um CMOS," IEEE Journal of Solid-State Circuits, 36(4):706-711.	
	0060	Esch and Manley, Theory and Design of CMOS HSTL I/O Pads, The Hewlett Packard Journal, Aug, 1998	
	0061	Xilinx, "Spartan-3 1.2V FPGA Family: Functional Description," Xilinx, DS099-2 (v1.2) July 11, 2003	
	0062	Xilinx, "Virtex-II 1.5V Field Programmable Gate Arrays," Xilinx, DSO3102 (v1.5), Apr. 2, 2001	
	0063	Xilinx, "Virtex-II Platform FPGAs: Detailed Description," Xilinx, DS031-2 (v3.1) October 14, 2003	
	0064	Xilinx, "Virtex-II Pro Platform FPGAs: Functional Description," Xilinx, DS083-2 (v2.9) October 14, 2003	

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